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Adiabatic Improved Efficient Charge Recovery Logic for Low Power CMOS Logic

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***Abstract* - Power dissipation becoming a limiting factor in VLSI circuits and systems. Due to relatively high complexity of VLSI systems used in various applications, the power dissipation in CMOS inverter, arises from its switching activity, which is mainly influenced by the supply voltage and effective capacitance. The low-power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit. One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and as parasitic. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching technique is use. Adiabatic switching is an approach to low-power digital circuits that differs fundamentally from other practical low-power techniques. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. When adiabatic switching is used, the signal energies stored on circuit capacitances may be recycled instead of dissipated as heat. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. Power reduction is achieved by recovering the energy in the recover phase of the supply clock.**

Keyword – CMOS, VLSI, Charge Recovery Logic.

I. Power Dissipation in CMOS circuits

Power dissipation in digital CMOS circuits can be classified into two types: dynamic power dissipation and static power dissipation. Dynamic power dissipation is due to high-to-low and low-to-high signal switching in circuits. Static power dissipation depends on the logic states of the circuit. It does not depend on signal switching. The average power dissipation in a digital CMOS circuit can be given by the following equation

$P_{avg} = P_{sw} + P_{sc} + P_{leak} + P_{static}$

Where, P_{sw} is the capacitive switching power dissipation, P_{sc} is the short-circuit power dissipation, P_{leak} is the power dissipation due to leakage currents and P_{static} is the static power dissipation due to non-leakage static currents. Capacitive switching power and short-circuit power are components of dynamic power dissipation. Leakage power is a major component of static power dissipation in CMOS circuits, though there might be some non-leakage currents that contribute to a small percentage of static power dissipation.

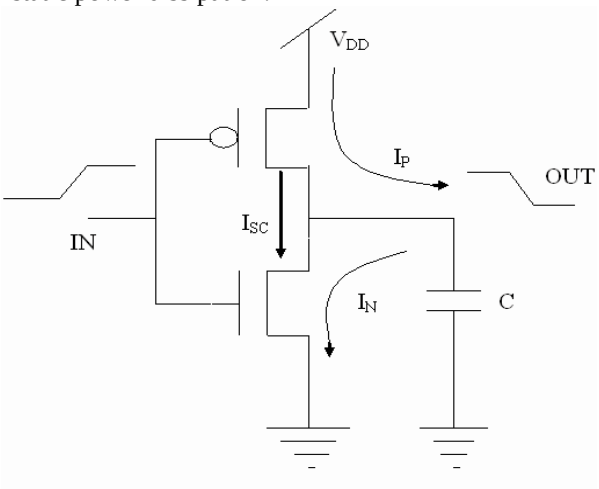


Fig.1. CMOS Inverter for Power Analysis.

II. Static Power Dissipation

Ideally, leakage power dissipation is the only source of static power dissipation in fully complementary digital CMOS circuits. In properly designed circuits non-leakage static currents can be avoided. Static power dissipation can however result from degenerated voltage levels at the inputs to static gates. Bus contention, signal conflicts due to multiple drivers, leakage current drawn continuously from the power supply also result in static power dissipation.

III. Dynamic Power Dissipation

Dynamic power dissipation is the most significant source of power dissipation in digital CMOS circuits and capacitive switching power is the largest contributor to dynamic power dissipation. Capacitive switching power is the power dissipation caused by charging and discharging of capacitances. In digital CMOS circuits, capacitances are formed from parasitic in the transistors and interconnection wires. These parasitic capacitances cannot be eliminated. Their estimation is crucial for dynamic power analysis and optimizations.

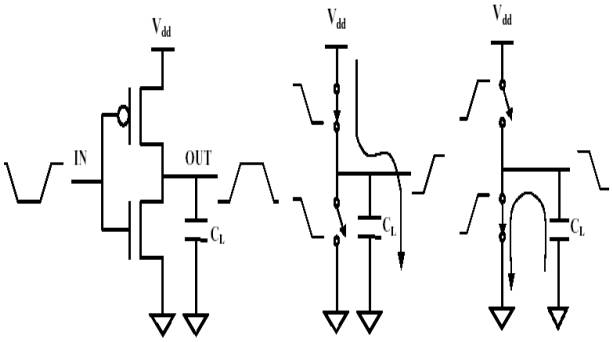
Consider the inverter in Fig.2 Assume that initially it is in steady state with input at logic HIGH and output at logic LOW. If there is a falling transition at the input from HIGH to LOW as shown in Figure 2 (a), then the

nmos transistor turns off while the pmos transistor turns on. The capacitance, C_L, is charged from the power supply. This charging process draws energy equal to CV_{DD}^2 from the power supply. Half of this is dissipated immediately in the PMOS transistors and the interconnect, while the other half is stored on the load capacitance. If the input undergoes a rising transition from LOW to HIGH as shown in Figure 2(b), then the pmos transistor turns off while the nmos transistor turns on. The capacitance C_L is completely discharged. The energy stored in the capacitor gets dissipated across the nmos and the interconnect. In summary, every time a capacitive node switches from ground to V_{DD} (and back to ground), energy of CV_{DD}^2 is consumed. This leads to the conclusion that CMOS power consumption depends on the *switching activity* of the signals involved. We can define *activity*, α as the expected number of zero to one transition per data cycle. If this is coupled with the average data rate, *f*, which may be the clock frequency in a synchronous system, then the effective frequency of nodal charging is given the product of the activity and the data rate: αf. This leads to the following formulation for the average CMOS power consumption:

$$P_{dyn} = a\, CV_{DD}^2 f$$

So, to reduce the power dissipation, the circuit designer can minimize the switching event, decrease the node capacitance, reduce the voltage swing or apply a combination of these methods. Yet, in all these cases, the energy drawn from the power supply is used only once before being dissipated. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching technique is use. Adiabatic switching is an approach to low-power digital circuits that differs fundamentally from other practical low-power techniques. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. When adiabatic switching is used, the signal energies stored on circuit capacitances may be recycled instead of dissipated as heat. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy. Power reduction is achieved by recovering the energy in the recover phase of the supply clock.

f specifies the number of times the capacitor charges and discharges in a given clock period. In an ideal synchronous circuit running at a clock frequency f the maximum rate of change of any signal will be f. Hence, the activity factor a will be a fraction between 0 and 1. The factor a is equal to the rate at which the capacitor C_L charges and discharges.



A B C

Fig.2. (A) CMOS Inverter (B) Charging Capacitor (C) Discharging Capacitor

IV. Short Circuit Power Dissipation

Short circuit power is a component of dynamic power dissipation in CMOS circuits. It is caused by the flow of short circuit current between supply and ground during switching or transition in signal values. Consider the inverter in Fig 2 Whenever there is a transition in the input signal, there is short duration in which the input signal is between the threshold voltages of the nmos and the pmos transistors and both transistors are turned on. This causes short circuit current to flow from supply to ground and results in short circuit power dissipation. If symmetric fall and rise times and threshold voltages are assumed, the short circuit power dissipation in a CMOS inverter can be approximately given by the following equation.

$$Psc = K.(Vdd - 2VT)\,3.t.N.f$$

Where, K is a constant that depends on the transistor sizes and the technology, VT is the magnitude of the threshold voltage of the nmos and pmos transistors, t is the input rise/fall time, N is number of transitions at inverter's output and f is the clock frequency.
Note that N = 2.a, where a is the activity factor.

V. Leakage Power Dissipation

Leakage power dissipation is a component of static power dissipation in CMOS circuits. It is caused by the presence of leakage currents in the MOS transistors. The major sources of leakage current in CMOS circuits are

i) Subthreshold channel conduction current.
ii) Gate Direct Tunneling Current
iii) Reverse Biased PN-junction current.

When a transistor is logically turned off, a non-zero leakage current flows through the channel. This happens when the gate voltage is below the threshold voltage. Hence, this leakage current is known as subthreshold leakage. Gate direct tunneling current occurs from tunneling of electrons or holes from the bulk and source or drain overlap region through the gate oxide potential barrier into the gate or vice-versa. The tunneling current increases exponentially with the decrease in the oxide

thickness and with increase in the potential drop across oxide.

VI. Principle of Adiabatic Switching

The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS.* Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source as shown in Fig. 3. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp. The energy dissipation in conventional CMOS circuits is caused by the channel resistance of the transistor. The dissipation through the channel resistance R is then:

$$\begin{aligned} E_{diss} &= P*T \\ &= I^2*R*T \\ &= (C*Vdd/T)^2\, RT \\ &= (2RC/T)CVdd^2 \end{aligned}$$

Thus we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply. Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies.

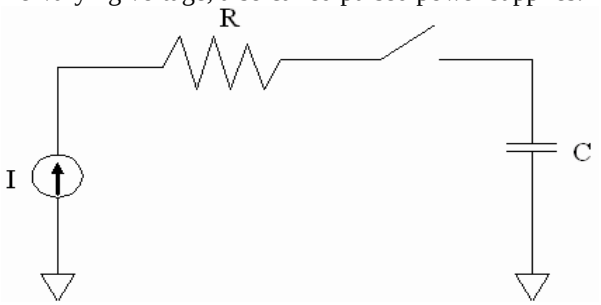


Fig.3. Circuit explaining Adiabatic Switching.

VII. Adiabatic Logic Circuits

Practical adiabatic families can be classified as either Partially adiabatic IC or fully adiabatic. In partially adiabatic circuits, some charge is allowed to be transferred to the ground, while in a fully adiabatic circuits, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization. Partially Adiabatic families include the following: Efficient Charge Recovery Logic (ECRL), Improved Efficient Charge Recovery Logic (IECRL), 2N-2N2PAdiabatic Logic, Positive Feedback Adiabatic Logic (PFAL), NMOS Energy Recovery Logic (NERL), Clocked Adiabatic Logic (CAL), True Single-Phase Adiabatic Logic (TSEL) and Source-coupled Adiabatic Logic (SCAL).

Some Fully adiabatic logic families include: Pass transistor Adiabatic Logic (PAL). Split- Rail Charge Recovery Logic (SCRL).

VIII. Results

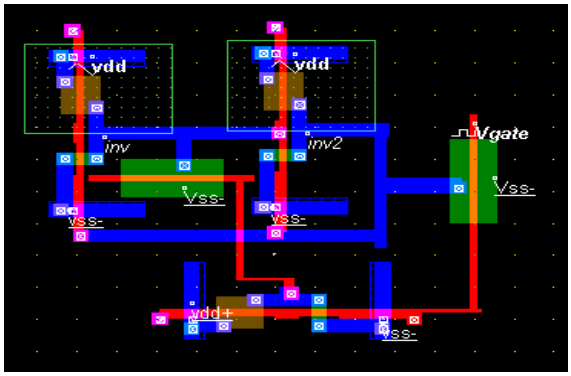


Fig.4. Adiabatic Inverter logic

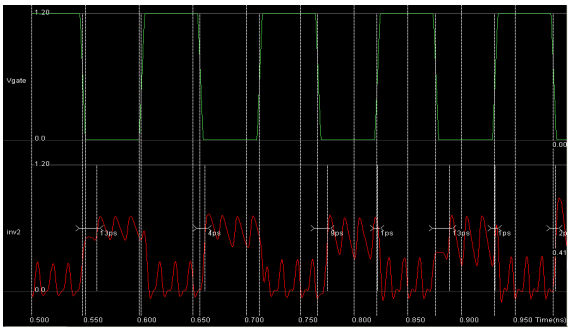


Fig.5. Adiabatic Inverter logic IECRL voltage v/s time

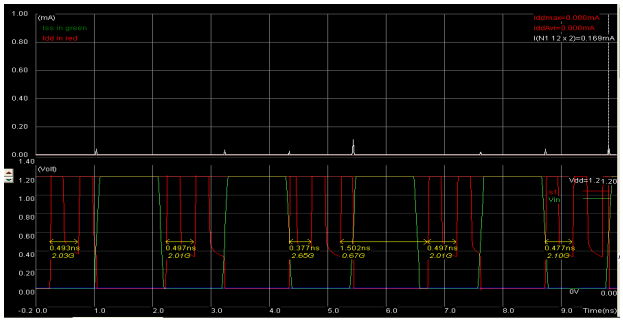


Fig.6. Adiabatic Inverter voltage and current

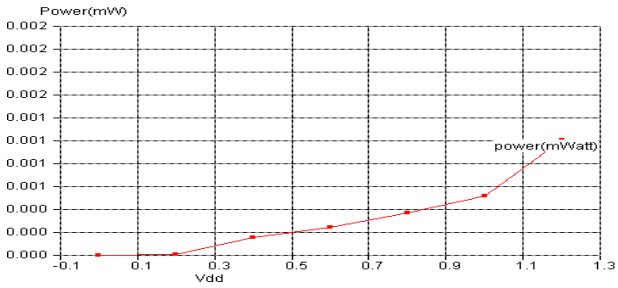


Fig.7. Adiabatic Inverter power dissipation from supply to output (1 uW)

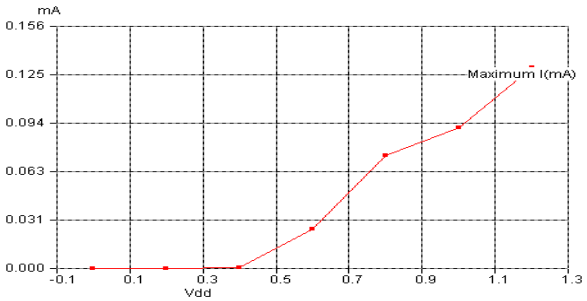


Fig.8. Adiabatic Inverter maximum current from supply to output (0.130mA).

Improved Efficient Charge Recovery Logic (IECRL), improves ECRL with the addition of a pair of cross-coupled NMOS devices. This produces a logic family that is based around a pair of cross-coupled inverters, a structure that is identical to the storage elements in a Static RAM (SRAM). The cross-coupled NMOS devices are an improvement over ECRL because they provide a pull down path to ground that remains even after the charge is recovered from the gates of the evaluation FETs. However, because of the two extra NMOS devices, it will require a larger area in which to be implemented. Fig 4 shows an inverter/buffer (also in buffer configuration) implemented using the IECRL style. Fig. 7 and Fig. 8 shows the energy dissipation in LPAL inverter. It may be noted that energy is being recovered after every input cycle.

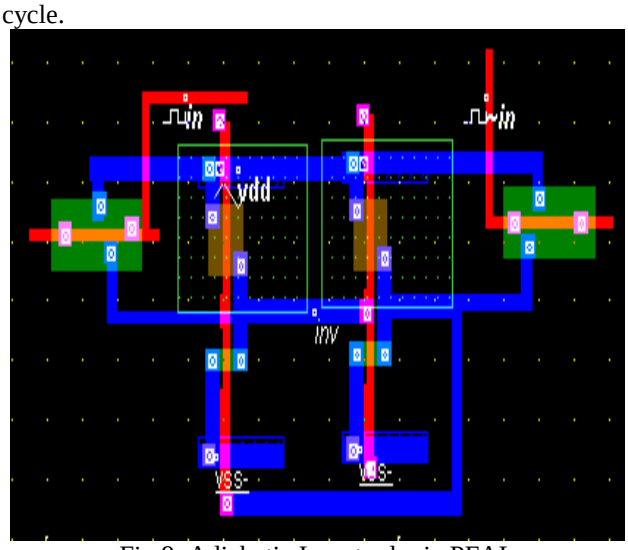


Fig.9. Adiabatic Inverter logic PFAL

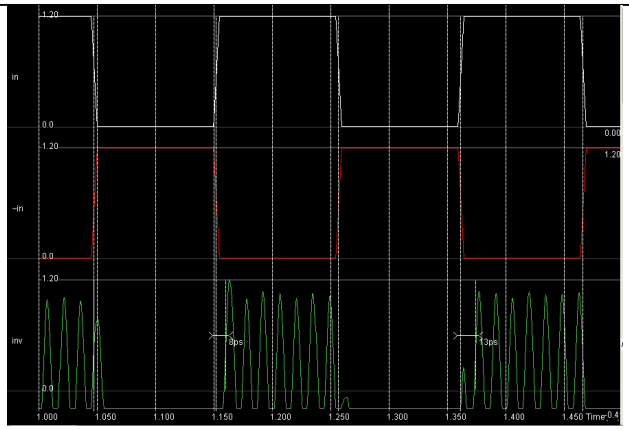


Fig.10. Adiabatic Inverter logic PFAL voltage v/s time

IX. Positive Feedback Adiabatic Logic (PFAL)

PFAL, like IECRL, is also based around a pair of cross coupled inverters. However, whilst in IECRL the NMOS devices used to evaluate the function are connected between the outputs and ground, in PFAL, these evaluation NMOS devices are connected between the outputs and the power-clock. The similarities between PFAL and IECRL gates are such that IECRL gates can be easily converted into PFAL gates. This is done by re-labeling the outputs so that their assertion levels are swapped, and connecting the NMOS evaluation devices between the power-clock and the outputs rather than between ground and the outputs. This can be made as easy to achieve in layout as it is in abstract representations of the circuit. When the power-clock is in its recovery phase, the NMOS devices between the outputs and the power-clock can allow complete recovery of those outputs. This means that the low-power performance of PFAL can be enhanced by making it fully reversible Fig 9 and Fig 10 shows an inverter/buffer implemented in the PFAL style.

X. Conclusion

Power reduction is achieved by recovering the energy in the recover phase of the supply clock.

If input changes from zero to Vdd, the voltage drops abruptly across the load capacitor and ground through NMOS. Adiabatic logic achieves low power by maintaining small potential differences across the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled. A power-clock supply plays an important role in adiabatic switching. When it ramps up or down steadily, the power-clock supply causes a very small drop across the switching device. The power-clock supply not only supplies the energy but also recovers it. Adiabatic inverters are the simplest form of benchmark circuit to demonstrate the principle of energy recovery and the adiabatic principle.

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